REMARKS/ARGUMENTS

Claims 15, 27, 35-39 and 41 are in the application, of which claims 15, 27 and 37 are the independent claims. Claims 1-14, 16-26, 28-34 and 40 were previously canceled. No claims are added, canceled, or amended herein. No new matter is believed to have been introduced to the application by this paper. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC §103

Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kajiwara et al. (U.S. Publication 2003/0127747, hereinafter "Kajiwara") in view of Hikita et al. (U.S. Publication 2003/0146518, hereinafter "Hikita"). **Claim 35** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Hikita, as applied to claim 15, and further in view of Dass et al. (U.S. Patent 6,162,652, hereinafter "Dass"). **Claims 27 and 37-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Fan et al. (U.S. Patent 6,956,292, hereinafter "Fan"), and Hikita. **Claims 36 and 41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Fan and Hikita, as applied to claims 27 and 37 above, and further in view of Dass. **Claim 39** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara in view of Fan and Hikita, as applied to claim 37 above, and further in view of Zhang et al. (U.S. Patent 6,104,461, hereinafter "Zhang"). Reconsideration and withdrawal of these rejections are respectfully requested.

Claim 15 is drawn to a method for fabricating a circuit component. The method includes the step of providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes the step of providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical

exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. The method further includes the step of, after said providing said exposed metallization structure, performing a sputter etching process with an argon gas.

Claim 27 is drawn to a method for fabricating a circuit component. The method includes the step of providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer over said semiconductor wafer and on said second region, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes the step of providing an exposed metallization structure over said semiconductor wafer, over said passivation layer and on said first region, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. The method also includes the step of, after said providing said exposed metallization structure, performing an ion milling process with an argon gas.

Claim 37 is drawn to method for fabricating a circuit component. The method includes the step of providing a semiconductor wafer, a metal pad over said semiconductor wafer, wherein said metal pad has a sidewall and a top surface with a first region and a second region between said first region and said sidewall, and a passivation layer on said second region and over said semiconductor wafer, wherein an opening in said passivation layer is over said first region, and said first region is at a bottom of said opening. The method also includes the step of providing an exposed metallization structure directly on said passivation layer, on said first region and over said semiconductor wafer, wherein said exposed metallization structure is connected to said first region through said opening, wherein said exposed metallization structure comprises a metal bump configured for a package interconnect, wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. The method also includes the step of, after said providing said exposed metallization structure, performing an ion milling process with an inert gas.

The applied references are not seen to disclose or suggest the foregoing combination of features of each of independent Claims 15, 27 and 37.

In this regard, the Office Action includes the assertion that "Kajiwara fails to explicitly disclose wherein said metal bump has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. However, Hikita [Fig. 1] discloses a method for fabricating a circuit component wherein said metal bump [3] has a substantially vertical exposed sidewall extending from a bottom of said metal bump to a substantially planar exposed top surface of said metal bump. Hikita discloses and makes obvious the suitable alternatives of various shapes of metal bumps. Because both references teach methods of forming metal bumps for external electrical connection in a semiconductor device, it would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable results of having the suitable bump design for the required device manufacturing process." *See* the Office Action, pg. 3, lines 8-18 with respect to claim 15, and pg. 6, lines 1-11 with respect to Claims 27 and 37-38.

Applicants respectfully disagree with this assertion. Kajiwara teaches that Au bump 7 is formed on Al electrode pad 4 by a ball bonding method using supersonic hot press bonding. *See* Kajiwara, ¶ [0039], lines 29-31. Kajiwara's ball bonding method would cause contamination of Au bump 7 and, thus, Kajiwara teaches that a surface cleaning treatment is performed to sputter etch a surface of Au bump 7. *See* Kajiwara, ¶ [0039], lines 40-45. Hikita, however, teaches the use of an electroplating or electroless plating method using oxidation-resistant metals, such as Au, Pd, Pt, Ag and Ir, instead of a ball bonding method to deposit metal bump 3. Hikita's electroplating or electroless plating method is not seen to contaminate metal bump 3 such that a surface cleaning treatment, such as Kajiwara's sputter etching process, would be required to clean the surface of metal bump 3. Accordingly, Kajiwara's surface cleaning treatment would not be considered for use on Hikita's metal bump 3, because no such cleaning would be required.

Accordingly, the teachings of Kajiwara and Hikita are not seen to disclose or make obvious the steps of "*performing a sputter etching process with an argon gas*" as recited in Claim 15 or "*performing a sputter etching process with an argon gas*" as recited in claims 27 and 37.

In view of the above, independent Claims 15, 27, and 37 are believed to be allowable over the applied references. Reconsideration and withdrawal of the rejections of Claims 15, 27, and 37 are therefore respectfully requested.

The other claims currently under consideration in the application are dependent from the independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the Amendments and Remarks herein, Applicants submit that the application is in condition for allowance and respectfully request a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,
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